EXHIBIT J

U.S. Patent No. 7,009,226

TSMC Products
(TSMC 28nm LP and 40nm Technology nodes)

U.S. Patent No. 7,009,226: Claim 1

"1. A semiconductor device comprising:"

1. A semiconductor device comprising:	Integrated circuits fabricated by TSMC in its 28nm LP or 40nm technology nodes (the "TSMC Products") include a semiconductor device. For example, the Qualcomm MSM8952 integrated circuit (the "Qualcomm Chip") is an exemplary TSMC Product.  *See e.g.*, TSMC28LP_001. The Qualcomm Chip is manufactured using TSMC's 28nm LP technology node. **Qualcomm Snapdragon 617 MSM8952**  The **Qualcomm Snapdragon 617 MSM8952** is a mid-range ARMv8-based SoC largely for Android tablets and smartphones announced in September 2015. In addition to 8 Cortex-A53 CPU cores at up to 1.5 / 1.2 (performance and power saving cluster) GHz, the SoC integrates an Adreno 405 GPU with a LPDDR3-1866 memory controller and supports Wi-Fi (802.11ac), Bluetooth 4.0, UMTS, and LTE. Compared to the older Snapdragon 615, the clock speeds are a bit lower (hits 1.7 GHz max). *See e.g.*, https://www.notebookcheck.net/Qualcomm-Snapdragon-617-MSM8952-SoC.156364.0.html.

U.S. Patent No. 7,009,226: Claim 1

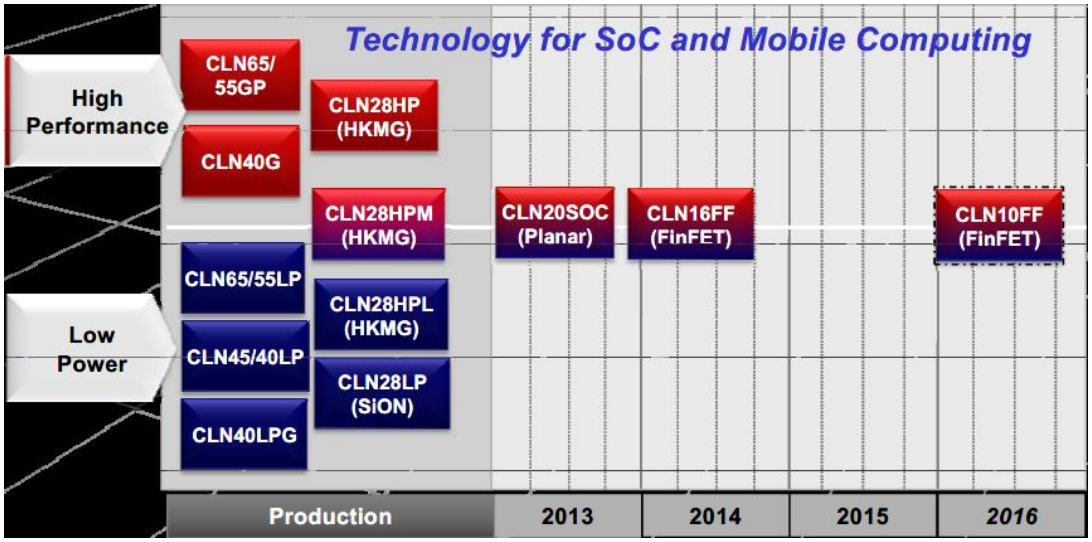
"1. A semiconductor device comprising:"

Power Consumption

The Snapdragon 617 is manufactured by TSMC in a 28 nm LP process. According to the specifications, we expect a medium or medium-high power consumption for use in medium-sized or larger smartphones and tablets.

See e.g., https://www.notebookcheck.net/Qualcomm-Snapdragon-617-MSM8952-SoC.156364.0.html.

TSMC's 28 nm technology platform is offered in four variants, denoted High Performance (HP), High Performance Mobile Computing (HPM), High Performance Low Power (HPL), and Low Power (LP). The LP technology node uses the SiON/Poly-Si gate stack.



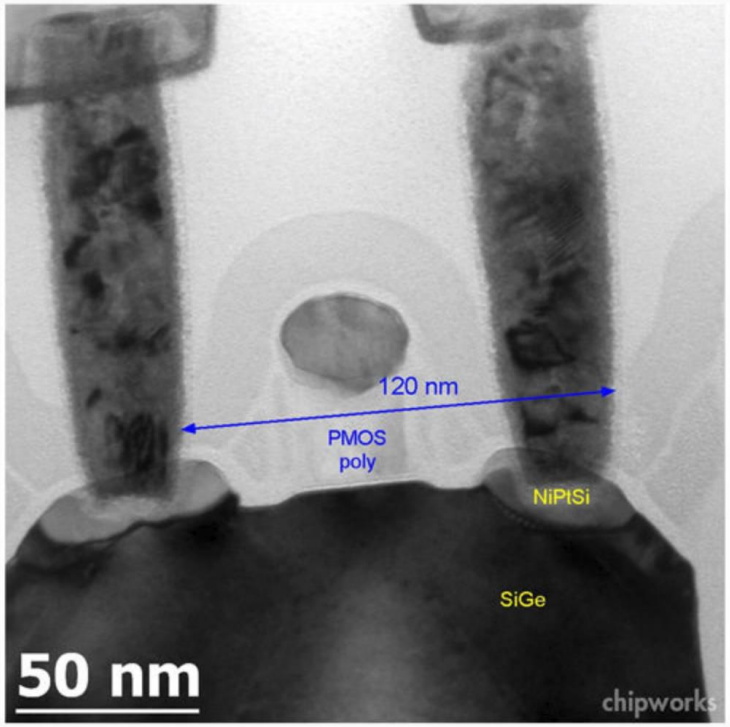
See Henry Hsieh, TSMC Technology and Innovation Platform for Mobile Computing (Nov., 2012), p.3, *available at* http://www.armtechforum.com.cn/2012/10_TSMC.pdf; TSMC, TSMC 28nm Technology in Volume Production, *available at* https://www.tsmc.com/uploadfile/ir/BusinessRelease/20111024161709877_sw3I/Oct24_2011_E.pdf.

TSMC's 28nm LP technology node is essentially a die shrink of TSMC's 40nm LP technology node.

U.S. Patent No. 7,009,226: Claim 1

"1. A semiconductor device comprising:"

The minimum contacted gate pitch was 120 nm. The 28 nm LP process is essentially a shrink of TSMC's 40 nm LP process (with the addition of the e-SiGe for PMOS), which was (notably) used to fabricate the NVIDIA Tegra T20-H-A2 application processor. The 40 nm LP process featured a 160 nm contacted gate pitch in the logic regions.

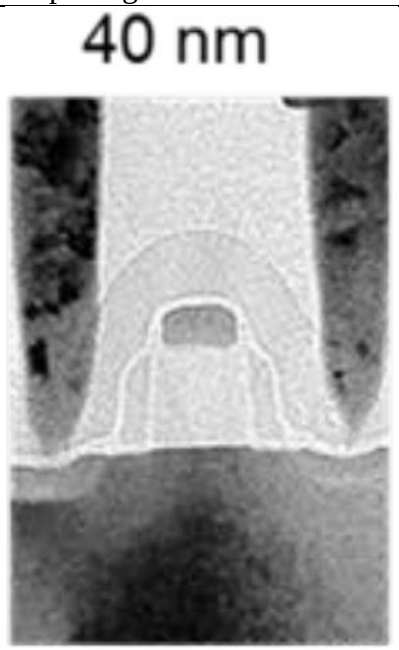


Qualcomm MSM8960 28 nm LP Snapdragon S3 Transistor Gate - TEM

See e.g., https://www.chipworks.com/about-chipworks/overview/blog/review-tsmc-28-nm-process-technology.

U.S. Patent No. 7,009,226: Claim 1

"1. A semiconductor device comprising:"



See e.g., TechInsights, Logic Roadmap, p.7, https://www.techinsights.com/techservices/TechInsights-Logic-Roadmap-2016.pdf.

Accordingly, the structure, function, operation, and implementation of integrated circuits fabricated on TSMC's 28nm LP technology node are substantially similar to the structure, function, operation, and implementation of integrated circuits fabricated on TSMC's 40nm technology node.

The TSMC Product comprises a semiconductor device. For example, the Qualcomm Chip includes a semiconductor device.

U.S. Patent No. 7,009,226: Claim 1

"1. A semiconductor device comprising:"

TSMC was founded in 1987 and is the world's largest foundry with 2011 revenues reaching $14.5 billion. According to their web site their total manufacturing capacity in 2011 was 13.2 million eight-inch wafer equivalents. They presently offer the full range of CMOS technologies from >0.5 µm down to 28 nm.

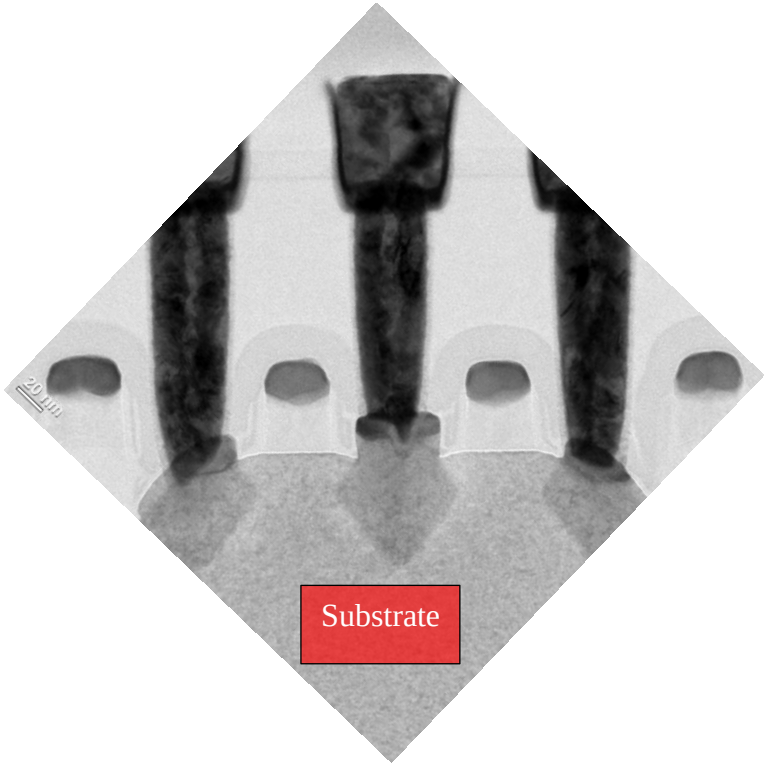
The 28 nm technology platform appeared in production in 2010 and is offered in four process variants, denoted HP, HPM, HPL and LP. We have analyzed three of these process variants to date, namely HP, HPL and LP. The 28 nm generation was the first time TSMC used high-k metal gate (HKMG) transistors. The HP and HPL technologies feature HKMG transistors, while the LP uses conventional poly gates, with an ONO gate dielectric. TSMC claims that their 28 nm process technology entered production in 2010; however, production devices were not available for analysis until mid-2011.

Standard Offerings		HP	HPM	HPL	LP
Core Vcc (V)		0.85	0.9	1.0	1.05
VT	Ultra-Low	✓	✓	✓	
	Low	✓	✓	✓	✓
	Standard	✓	✓	✓	✓
	High	✓	✓	✓	
	Ultra-High		✓		
1.8V I/O	1.8V UD 1.2V	✓	✓		✓
	1.8V UD 1.5V	✓	✓	✓	✓
	1.8V	✓	✓	✓	✓
2.5V I/O	2.5V UD 1.8V	✓	✓	✓	✓
	2.5V	✓	✓	✓	✓
	2.5V OD 3.3V	✓	✓	✓	✓
SRAM	SP	✓	✓	✓	✓
	DP	✓	✓	✓	✓

See e.g., https://www.chipworks.com/about-chipworks/overview/blog/review-tsmc-28-nm-process-technology.

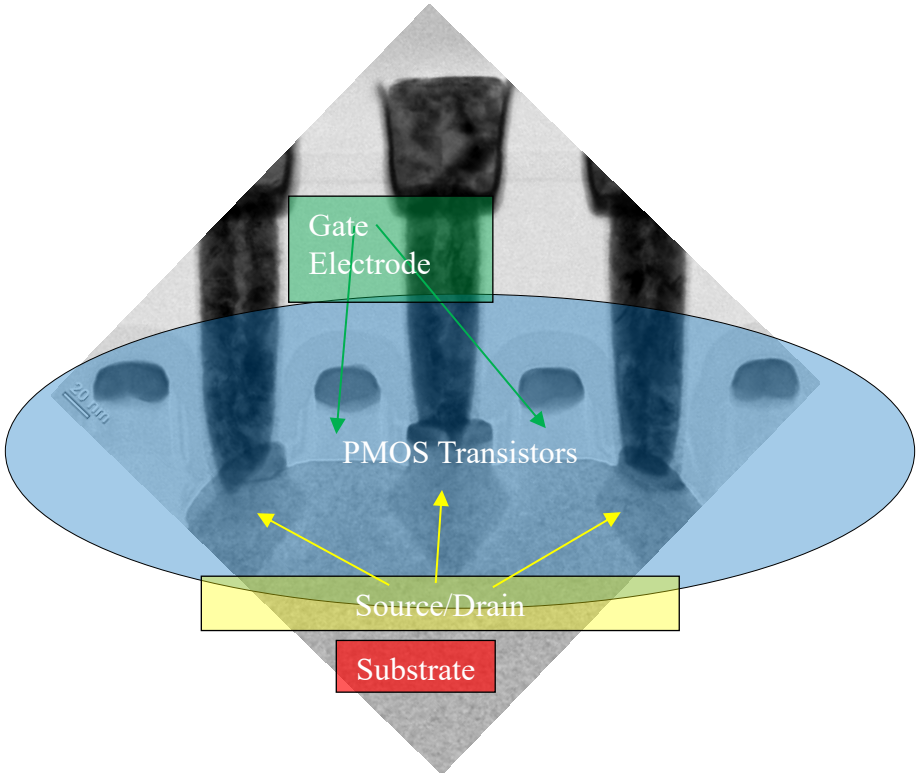
U.S. Patent No. 7,009,226: Claim 1

"a substrate;"

a substrate;	The TSMC Product includes a substrate. For example, a typical PMOS transistor is located on a substrate.  *See e.g.*, TSMC28LP_009.

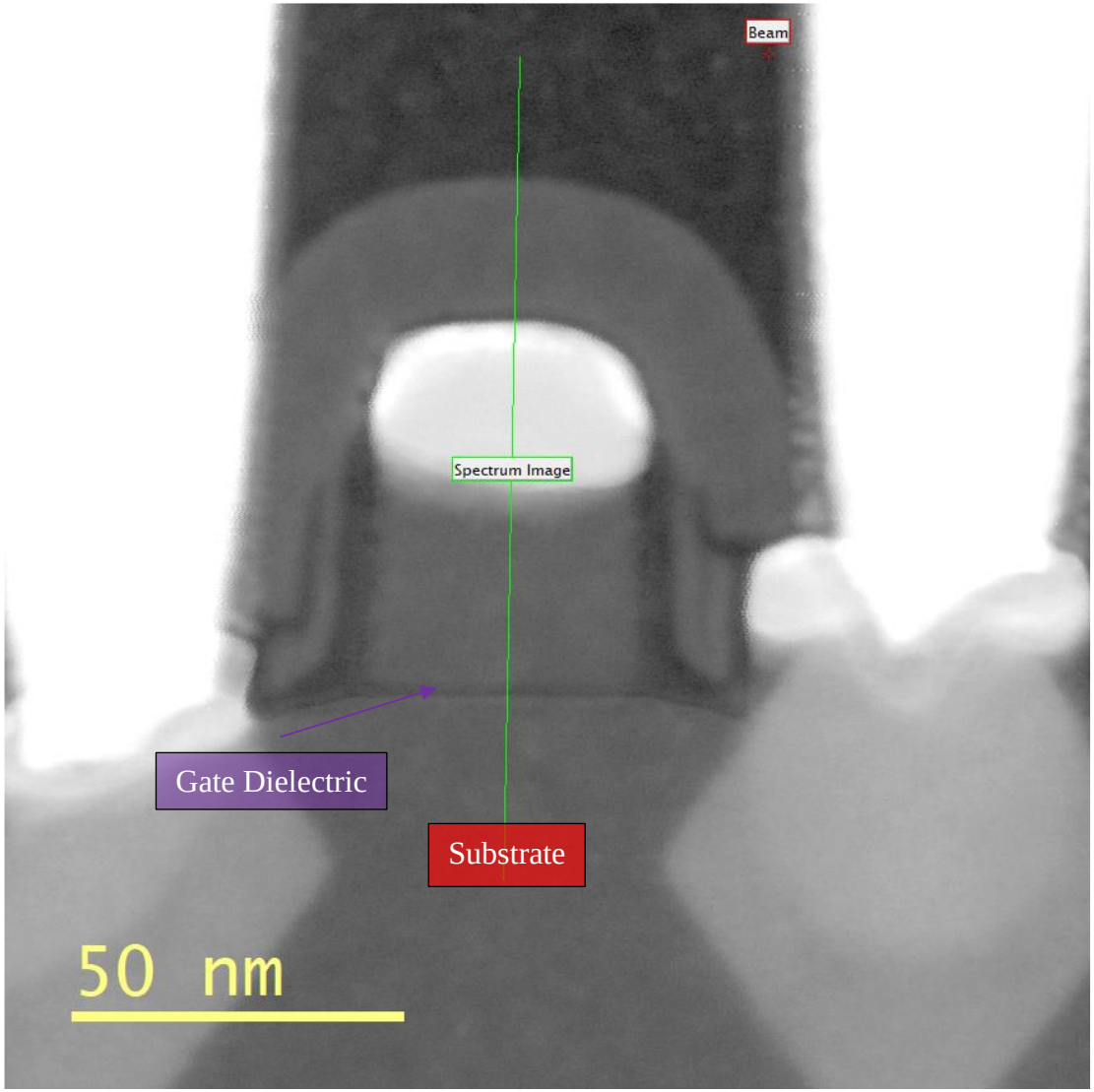
U.S. Patent No. 7,009,226: Claim 1

" a plurality of transistors formed on the substrate, each transistor comprising source/drain regions and a gate electrode, having an upper and side surfaces, over the substrate with a gate dielectric layer therebetween, the gate electrodes being separated by a gap;"

a plurality of transistors formed on the substrate, each transistor comprising source/drain regions and a gate electrode, having an upper and side surfaces, over the substrate with a gate dielectric layer therebetween, the gate electrodes being separated by a gap;	The TSMC Product includes a plurality of transistors formed on the substrate, each transistor comprising source/drain regions and a gate electrode, having an upper and side surfaces, over the substrate with a gate dielectric layer therebetween, the gate electrodes being separated by a gap. For example, the Qualcomm Chip includes multiple PMOS transistors that include source/drain regions and gate electrodes. Typical PMOS transistors as used in the Qualcomm Chip are pictured below. The PMOS transistors are formed over the substrate and include source/drain regions and gate electrodes with upper and side surfaces. The gate electrodes are separated by a gap.  *See e.g.*, TSMC28LP_009. The transistors formed on the substrate with a gate dielectric layer therebetween. For example, the Qualcomm Chip includes transistors that are formed on the substrate and separated from the substrate by a gate dielectric. Electron Energy Loss Spectroscopy (EELS) samples along the gate region show the presence of Si and O in the gate dielectric as reflected by the below diagram.

U.S. Patent No. 7,009,226: Claim 1

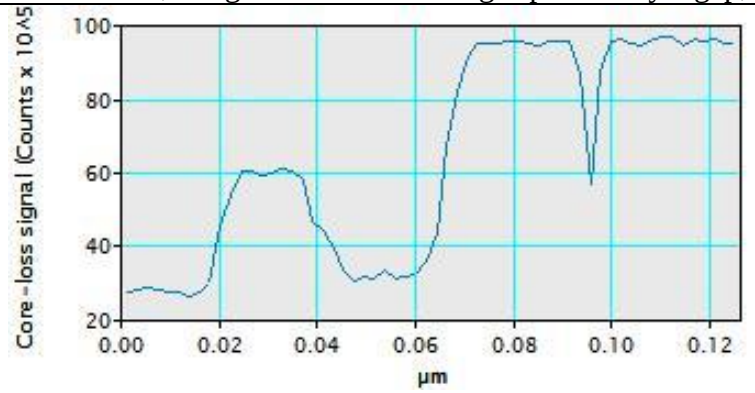
" a plurality of transistors formed on the substrate, each transistor comprising source/drain regions and a gate electrode, having an upper and side surfaces, over the substrate with a gate dielectric layer therebetween, the gate electrodes being separated by a gap;"



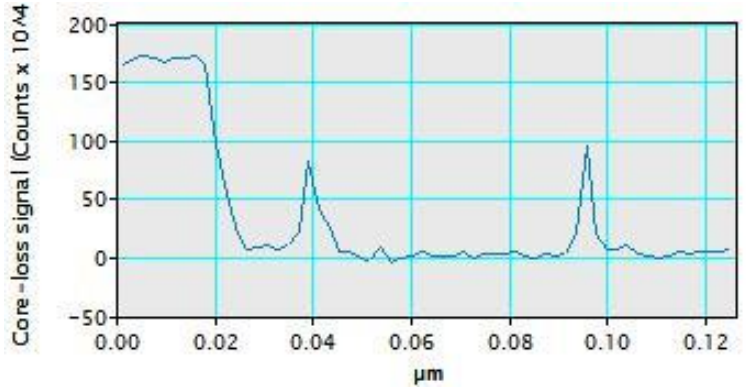
See e.g., TSMC28LP_010.

U.S. Patent No. 7,009,226: Claim 1

" a plurality of transistors formed on the substrate, each transistor comprising source/drain regions and a gate electrode, having an upper and side surfaces, over the substrate with a gate dielectric layer therebetween, the gate electrodes being separated by a gap;"



See e.g., TSMC28LP_011.



See e.g., TSMC28LP_012.

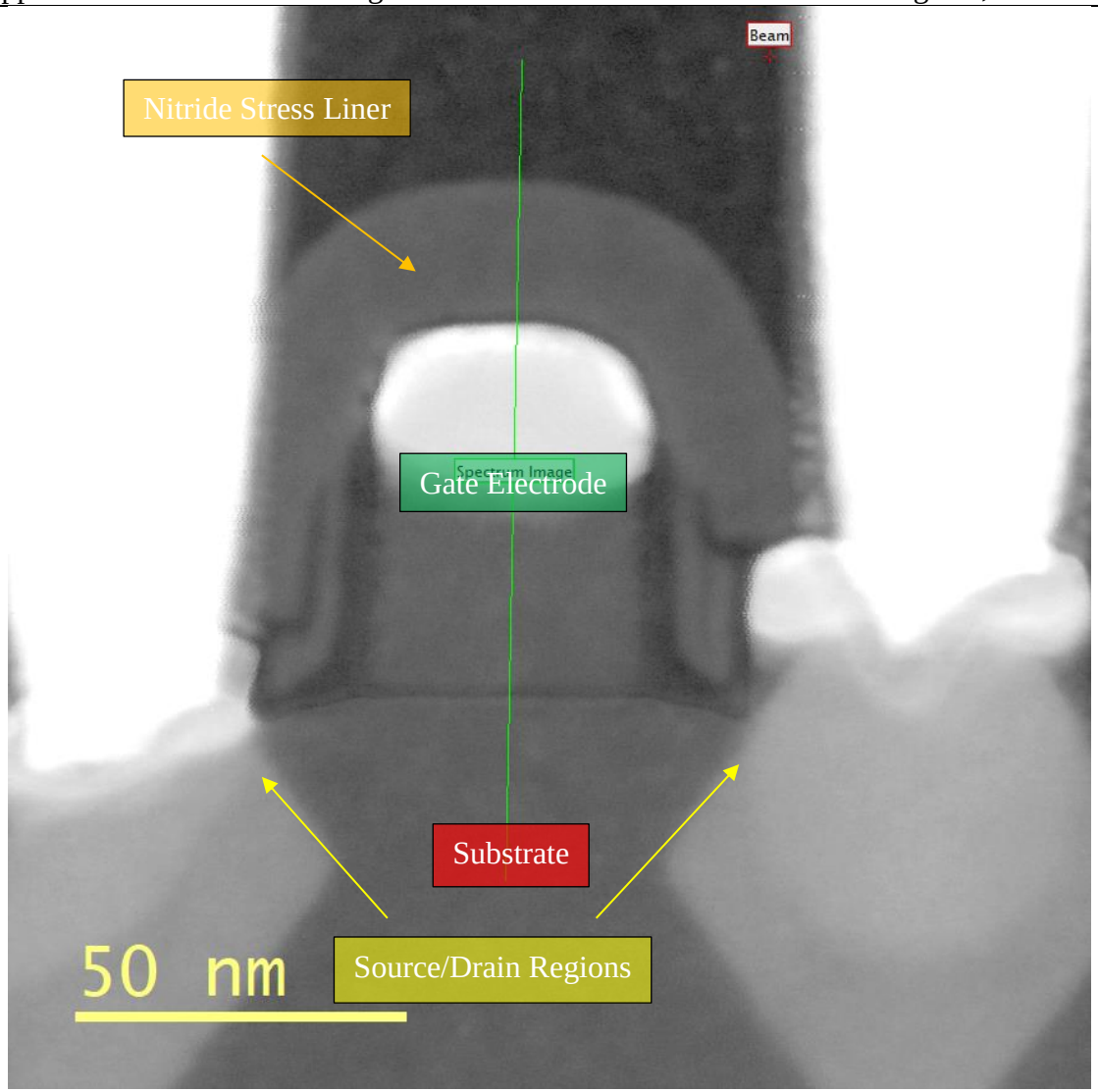
U.S. Patent No. 7,009,226: Claim 1

" a conformal stressed nitride liner over the upper and side surfaces of the gate electrodes and over the source/drain regions; and "

a conformal stressed nitride liner over the upper and side surfaces of the gate electrodes and over the source/drain regions; and	The TSMC Product comprises a conformal stressed nitride liner over the upper and side surfaces of the gate electrodes and over the source/drain regions. For example, the Qualcomm Chip includes a PMOS transistor that further includes a conformal stressed nitride liner. The conformal stressed nitride liner is over the upper and side surfaces of the gate electrodes and over the source/drain regions. Electron Energy Loss Spectroscopy (EELS) samples along the stress liner region show the presence of N and Si in the stress liner as reflected by the below diagram.

U.S. Patent No. 7,009,226: Claim 1

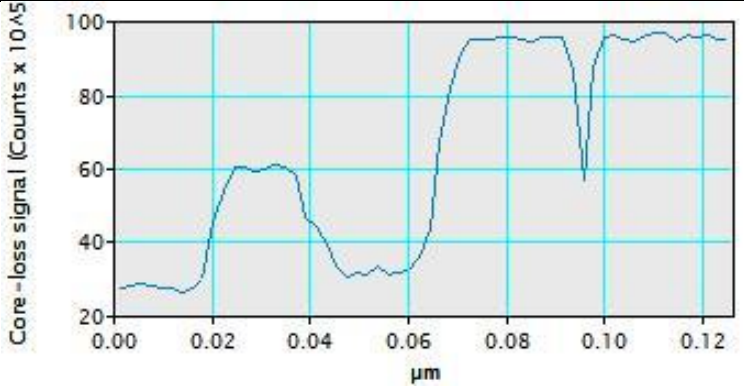
" a conformal stressed nitride liner over the upper and side surfaces of the gate electrodes and over the source/drain regions; and "



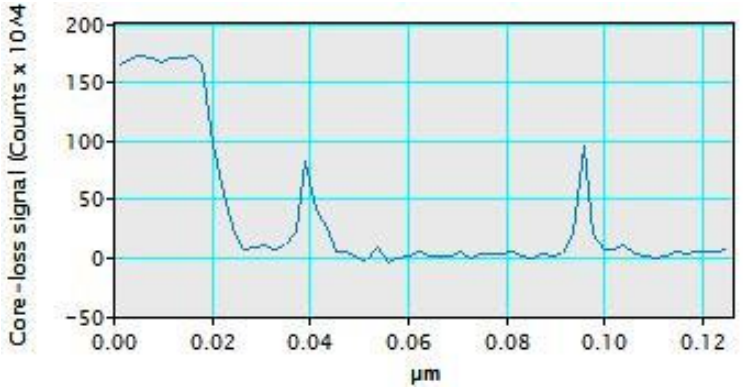
See e.g., TSMC28LP_010.

U.S. Patent No. 7,009,226: Claim 1

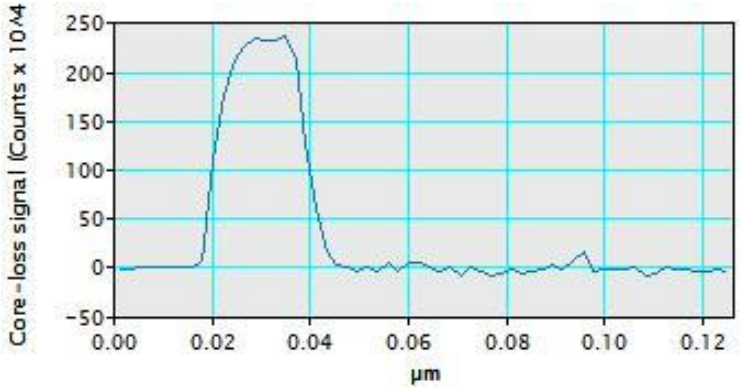
" a conformal stressed nitride liner over the upper and side surfaces of the gate electrodes and over the source/drain regions; and "



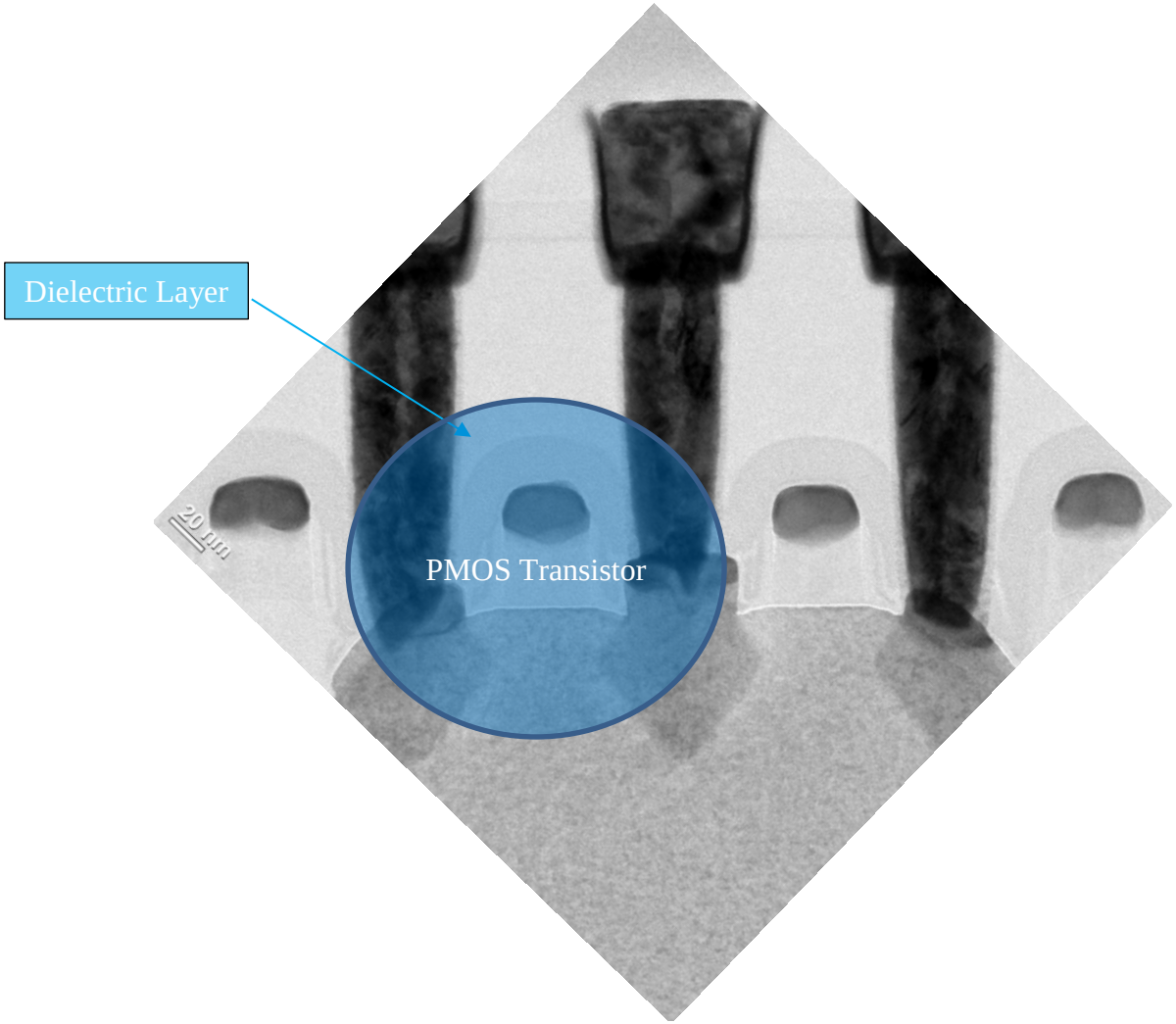
See e.g., TSMC28LP_011.

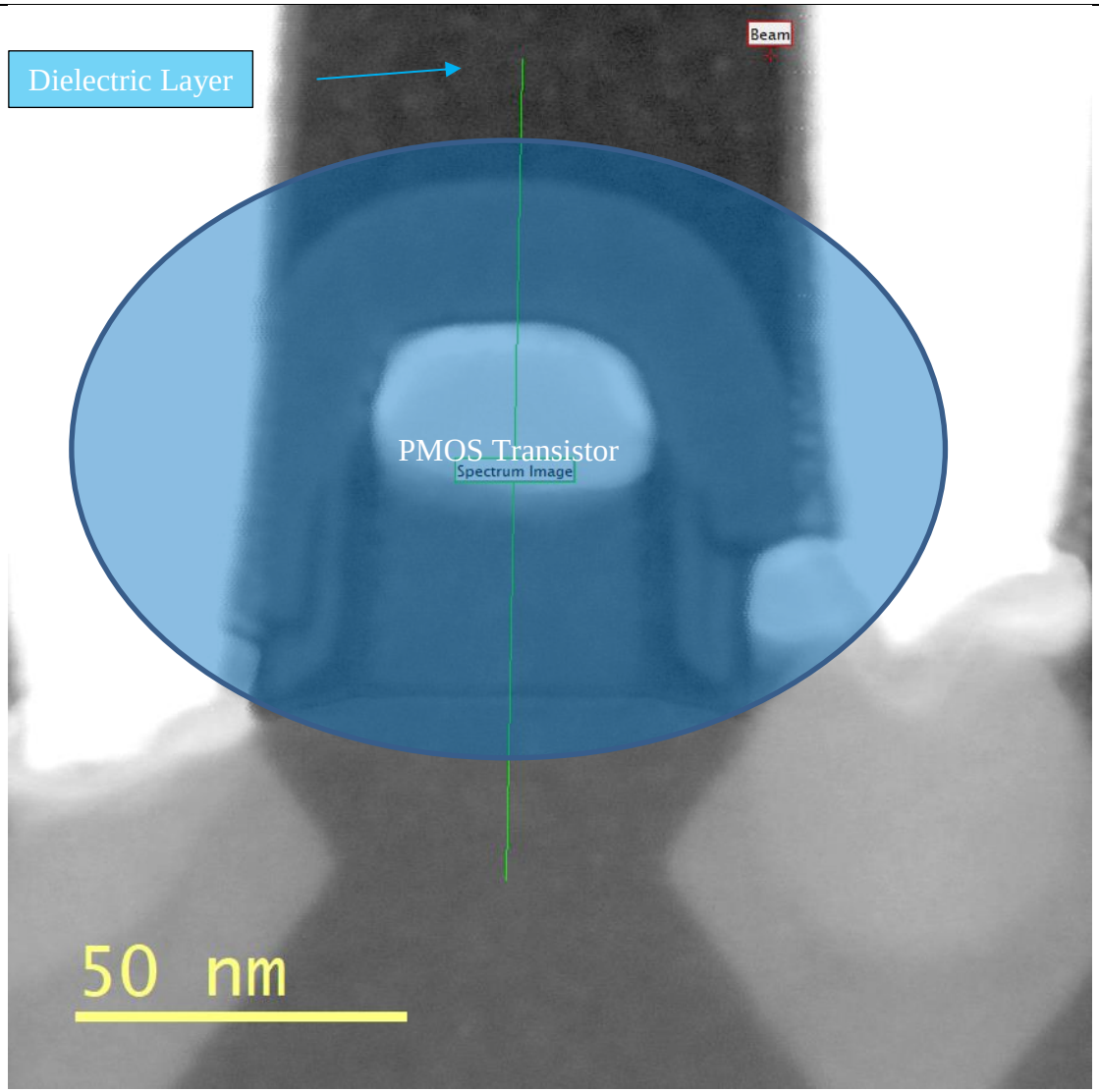


See e.g., Qualcomm TSMC28LP_012.

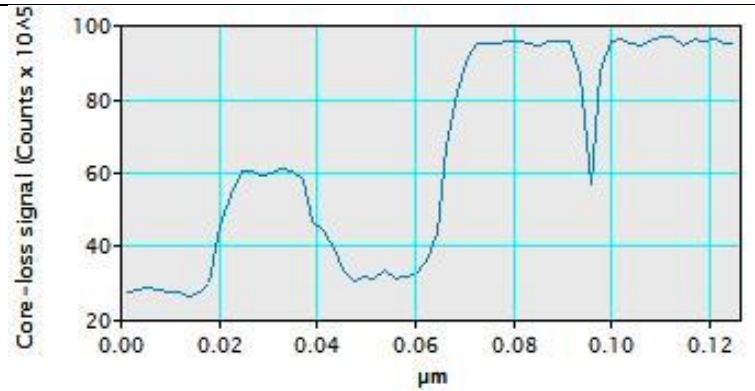


See e.g., Qualcomm TSMC28LP_013.

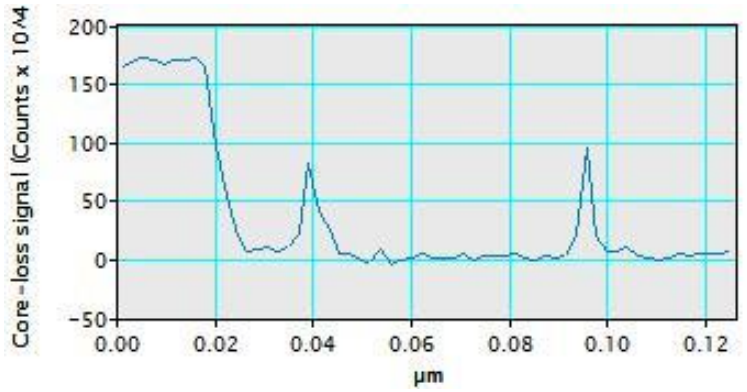
a dielectric layer over the transistors and filling the gaps between the gate electrodes.	The TSMC Product comprises a dielectric layer over the transistors and filling the gaps between the gate electrodes. For example, the Qualcomm Chip includes a dielectric layer over the transistors and filling the gaps between the gate electrodes. For example, EELS samples along the dielectric layer show the presence of Si and O in the dielectric layer as reflected by the below diagram.  *See e.g.*, TSMC28LP_009.



See e.g., TSMC28LP_010.



See e.g., TSMC28LP_011.



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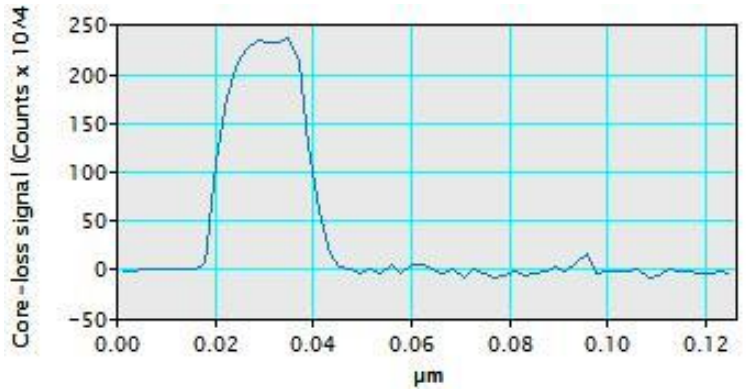

See e.g., TSMC28LP_013.